

METHOD OF AND SYSTEM FOR ANALYZING CELLS OF A MEMORY DEVICE

ABSTRACT

A method of analyzing cells of a memory device is disclosed. The method generally comprises steps of establishing a plurality of fail signatures, wherein each fail signature is associated with a type of failure. Voltages according to a plurality of test patterns are applied to nodes of a cell of the memory device. Fail data of the cell for the plurality of patterns is then analyzed, and a fail signature of the cell is determined. A type of failure of the cell based upon the plurality of fail signatures is then determined. A system for analyzing cells of a memory device is also disclosed. The system preferably comprises a plurality of probes applying different voltages to a cell of the memory device. A control circuit varies the voltages applied to the cell, and compares the failures of the cell as the test voltage applied to the cell is varied to an artificial bit map. Finally, an output device generates an output indicating a type of failure of the cell.